

Addis Ababa Science and Technology University
College of Engineering
Department of Electrical and Computer Engineering

Computer Architecture and Organization
Course Syllabus

Lecturer: Esubalew Mulat
September, 2019 E.C (Oct, 2026 G.C)

Course Information

Course Title:	Computer Architecture and Organization
Course Code:	ECEg4103
Credit Hours:	3 (2 Lecture, 3 Tutorial)
Target Group:	4th Year — Electrical and Computer Engineering
Semester:	I
Prerequisites:	Digital Logic Design (ECEg3104)
Lecturer:	Esubalew Mulat
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Office/Hours:	B-63/308 (Time TBN)

Course Description

This course provides an in-depth introduction to the **organization and architecture of computer systems**. Discussions will be made starting from the classic computers, progressing to more modern architectural designs. Students will gain both theoretical understanding and practical skills into how computers and their integral components are structured, designed and operate. The following are the core elements of the course:

I. Introduction and Historical Trends: Explore the fundamentals of computers, computer organization and architecture, the evolution of computing systems and performance measurement techniques. Students are expected to aprpeciate the importance of small steps in technological advancements.

II. Central Processing Unit (CPU): Study the heart of the computer, instruction sets, instruction formats, and addressing modes. Examine RISC and CISC architectures, pipelining, and the control unit. Hands-on experience with assembly and machine language programming will reinforce these concepts.

III. Memory Systems: Discussion about the fundamental design principles of memory units and their organization towards large size memory systems will be made.

IV. Input/Output Systems: Brief introduction to historical trends, types and interfaces of I/O computer technology will be made.

Course Learning Outcomes

No	CLO Code	CLO	Program Outcome
1	CLO 1	Explain the basic building blocks, the historical developments, and performance assessment of computers.	PO1
2	CLO 2	Explain the components, internal interconnections, and functions of computers.	PO2
3	CLO 3	Explain the structure, functions and operational elements of the central processing unit and its components.	PO1, PO2
4	CLO 4	Explain instruction set characteristics, functions, addressing modes and formats.	PO1, PO2
5	CLO 5	Explain the overall memory organization, and working principles of cache memory.	
6.	CLO 6	Explain internal memory (RAM) design principles.	PO2
7	CLO 7	Design small scale computers.	PO3, PO5, PO9, PO10

Course Contents

Chapter / Topic	Subtopics	CLO	Guided Learning (F2F)	Independen Learning (NF2F)	Total SLT
Chapter 1: Computer Evolution and Performance	1.1 Organization and Architecture 1.2 Structure and Function of Computer 1.3 History of Computer 1.4 Design for Performance 1.5 Performance Assessment	CLO1	1 1 1 1 1+1	2 2 2 2 1	3 3 3 3 3
Chapter 2: Top Level of Computer Function and Interconnection	2.1 Computer Components 2.2 Computer Functions 2.3 Interconnection Structures 2.4 Bus Interconnection	CLO2, CLO7	1 1 + 2 1 + 1 1 + 1	2 3 3 3	4 6 5 5
Chapter 3: Instruction Sets and Addressing Modes	3.1 Instruction Set Design 3.2 x86 and ARM Instruction Formats 3.3 Addressing Modes 3.4 x86 and ARM Addressing Modes 3.5 Assembly Language	CLO4, CLO7	1 + 1 1 1+1 1 2+3	3 3 3 3 1	4 4 5 4 6
Chapter 4: Processor Structure and Function	4.1 Processor Organization 4.2 Register Organization 4.3 Instruction Cycle 4.4 Instruction Pipelining 4.5 Control Unit	CLO3, CLO7	1 1 + 1 1 + 1 2 + 2 1	3 3 3 1 2	4 5 5 5 3
Chapter 5: Memory Systems	5.1 Computer Memory System Overview 5.2 Cache Memory Principles 5.3 Elements of Cache Memory Design 5.4 Semiconductor Memory Design 5.5 Error Correction in Memories	CLO5, CLO6	1 1 + 1 2 + 1 1 1	3 1 1 2 1	4 3 4 3 2
Chapter 6: I/O Module	6.1 External Devices 6.2 I/O Modules 6.3 Interrupt-driven I/O 6.4 Direct Memory Access 6.5 I/O Channels and Processors	CLO2	1 1 1 1 1	1 1 1 1 1	2 2 2 2 2

- ***Note:*** In **F2F** X represents Lecture Hrs, X + Y represents Lecture + Tutorial Hrs

Assessment Methods

No	Component	Weight	CLO
1	Individual Assignment	5%	CLO1
2	Midterm Exam	20%	CLO1-CLO3
3	Project	25%	CLO2-CLO4, CLO7
4	Final Exam	50%	ALL CLOs

Course Policy

Academic rules, regulations and policies (including the AI policy) of the university shall be followed in the course. Discussions will be made in Class!

References

1. **W. Stallings, Computer Architecture and Organization. 10th edition, Pearson, 2016.**
2. M. Mano, Computer System Architecture, 3rd edition, Prentice Hall, 1993.
3. V.C. Hamacher, Computer Organization, McGraw Hill,5th edition 2001.
4. J.P.Hayes, Computer Architecture and Organization, McGraw Hill,2012
5. J.L. Hennessy, D.A. Patterson, Computer Organization and Design, Morgan Kaufmann, 5th edition, 2013.
6. Books and course materials associated with recent GPUs, TPUs and chips used for AI works.